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EXAMINER
KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/353,120	VILLAROSA ET AL.	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-16,19-22,25 and 27-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7,10,16,19-22,27 and 28* is/are allowed.

6)☒ Claim(s) *11-13* is/are rejected.

7)☒ Claim(s) *14, 15, 25, 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments have been considered but is moot in view of the new ground(s) of rejection.

Response to Amendment

1. Claims 11, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamane et al. USPN 4965797.

1. Regarding claim 11, Yamane shows a method for detecting errors in the synchronization of a DTE data signal (Yamane fig. 4: output of 31: MD1) with a DCE clocking signal (Yamane fig. 4: phi1) in a communication environment wherein the DCE interfaces the DTE to a communication channel, the method comprising the steps of:

a. providing a master clock signal (Yamane fig. 4: phi0) ~~having a frequency that is an integer multiple of the frequency of the DCE clocking signal (Yamane fig. 4: input clock; fig. 9 shows multiple clock phi3 is at twice the frequency of the input clock)~~

b. deriving a ~~circuit~~ DCE clocking signal (Yamane fig. 4: bottom output of divider 34, phi1) and an internal clocking signal (Yamane fig. 4: phi2) from said master clocking signal (Yamane fig. 4: phi0), said ~~circuit~~ internal clocking signal (Yamane fig. 7: phi2) having the same frequency as the DCE clocking signal (Yamane fig. 7: phi1).

c. obtaining a first sample of said DTE data signal at a first time ~~based on said circuit clocking signal~~ (Yamane fig. 11m: D(0)) ~~and obtaining~~ a second sample of said DTE data signal at a second time ~~based on said master clocking signal~~ (Yamane fig. 11m:

D(1)), said second time being subsequent to said first time (Yamane fig. 11m: D(1) is after D(0)), the time interval between said first time and said second time being less than the period of the DCE clocking signal (Yamane fig. 11 m, n, d: the clock for clocking the MD1 data in m is in n which is at twice the frequency of the divided clock, d, which is the DCE clocking signal phi1)

d. comparing said first sample to said second sample (Yamane fig. 8: comparison of samples is occurring in 31 with the NAND gates)

e. and determining whether the DTE data signal has undergone a transition during the time interval between the first time and the second time. (Yamane fig. 10: comparison of samples is occurring in 49 with the NAND gates)

2. Claims 12 and 13 have not been amended and the prior rejections stand.

3. Claims 8, 9, 17, 18, 23, 24, 26 are cancelled.

Allowable Subject Matter

4. Claims 14, 15, 25 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claim 1 is allowed and thus claim 1's dependent claims are allowed which include: 2, 3, 4, 5, 16, 19, 20, 21, 22, 27 and 28.

6. Claim 6 is allowed and thus claim 6's dependent claims are allowed which include 7 and 10.

7. The following is a statement of reasons for the indication of allowable subject matter: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with the bolded portions:

8. As per claim 14, the method of claim 13, further comprising the steps of: inverting said circuit clocking signal to produce an inverted circuit clocking signal (discussed above); and ~~producing an output signal that is selected from the group selected from said circuit clocking signal and said inverted circuit clocking signal (not in Yamane)~~ ***producing an internal clocking signal that is selected in response to said selector control signal, from the group consisting of said DCE clocking signal and said inverted clocking signal.(not in Yamane)***

9. As per claim 29, the method of claim 13, further comprising the steps of: inverting said internal clocking signal to produce an inverted circuit clocking signal (discussed above); and ***producing said DCE clocking signal that is selected in response to said selector control signal, from the group consisting of said internal clocking signal and said inverted clocking signal. (not in Yamane)***

10. Claims 15 and 25 depend on claim 14 and thus claims 15 and 25 are also objected to.

11. Regarding claim 1, Yamane shows in figure 4, a circuit for detecting errors in the synchronization of a DTE data signal (Yamane fig. 10: output of 49) with a DCE clocking signal (Yamane fig. 4: input clock) in a communication environment wherein the DCE interfaces the DTE to a communication channel at an interface rate determined by the DCE clocking signal, the circuit comprising:

f. ~~a master clock producing~~ a clock generating circuit (Yamane fig. 4: 33, fig. 3: 33) configured to generate a master clock signal (Yamane fig. 4: multiple clock; fig. 10: phi3)

~~having a frequency that is an integer multiple of the frequency of the DCE clocking signal (Yamane fig. 4: input clock; fig. 9 shows multiple clock phi3 is at twice the frequency of the input clock; fig. 10 shows input clock phi0 is at fo while phi3 is at 2fo).~~

g. ~~a clock generator deriving (Yamane fig. 4: Divider 34)~~ a DCE ~~circuit~~ clocking signal ~~from said master clock signal (Yamane fig. 4: multiple clock), said circuit clocking signal (Yamane fig. 11: f divided clock) having the same frequency as the DCE clocking signal (Yamane fig. 11: a input clock; in fig. 11, a and f are at the same frequency)~~ and an internal clocking signal (Yamane fig. 4: bottom output of divider 34; fig. 10: phi1), each of the DCE clocking signal (Yamane fig. 4: input clock, phi0) and internal clocking signal having a first frequency that is a fraction of the frequency of the master clock signal; (Yamane fig.9 shows phi1 and phi0 at a fraction of the frequency of phi3)

h. a sample enable generator (Yamane fig. 10: 28) ***configured to receive the master clock signal and the internal clocking signal and to generate*** (not in Yamane) ~~for generating~~ a first sample enable signal (Yamane fig. 10: sel1) at a first time ~~related to said circuit clocking signal~~ and a second sample enable signal (Yamane fig. 10: sel2) at a second time ~~related to said master clock signal~~ (master clock, which is the output of 33, is related to the circuit clock, which is the output of 34, and both are used to obtain the sample enable signals) the second time being subsequent to the first time ; and

a sample comparator ~~for using~~ having inputs that receive said first sample enable signal, said second enable signal and said DTE data signal, the sample comparator configured to sample the DTE data signal at the first time and sample the DTE data signal at the second time, the sample

comparator further configured to compare the DTE data signal sample at the first time with the DTE data signal sample at the second time and determine from the comparison whether the DTE data signal has undergone a transition during the time interval between said first time and said second time (Yamane fig. 10: comparison of samples is occurring in 49 with the NAND gates).

12. Regarding claim 6, McMahan et al. shows in figure 1, a circuit for detecting and correcting clocking errors in the synchronization of a DTE data signal (McMahan 11) with a DCE clocking signal (McMahan 43 and 55) in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

i. Means for producing a master clock signal (McMahan HS CLK) ~~having a frequency greater than the frequency of the DCE clocking signal (McMahan: At the end of the first full paragraph of column 6, it is implied that the master clock signal is 16 MHz and the DCE clocking signal is 1.544 MHz;)~~

j. Means for deriving a ~~circuit~~ DCE clocking signal ***and an internal clocking signal*** (not in McMahan) from said master clocking signal, said ~~circuit~~ internal clocking signal having the same frequency as the DCE clocking signal. (a clock generator (McMahan 55) deriving a circuit clocking signal (TX CLOCK) from said master clock signal (McMahan HS CLK input to 48), said circuit clocking signal having the same frequency as the DCE clocking signal;)

k. means for obtaining a first sample of said DTE data signal at a first time (McMahan 15) and a second sample of said DTE data signal at a second time (McMahan 15), said second time being subsequent to said first time, the interval between said first time and said second time being less than the period of the DCE clocking signal. As

indicated in the first office action, the interval between the first and second time is 1/(16 MHz), which is less than 1/(1.544MHz), the period of the DCE clocking signal

l. means for comparing said first sample to said second sample (McMahan 21)

m. means for generating a selector control signal if said first sample is different from said second sample (McMahan 23)

n. means for inverting said ~~circuit~~ internal clocking signal to produce an inverted ~~circuit~~ clocking signal (McMahan fig. 2: 203 and 205; col. 5 lines 55 to 60); and

o. means for selecting, in response to said selector control signal, an output signal from the group consisting of said ~~circuit~~ internal clocking signal and said inverted circuit clocking signal (McMahan fig. 2: selects between 203 and 205) ~~in response to said selector control signal (McMahan fig. 1: the appropriate TX CLOCK is selected in response to 23)~~.

13. Regarding claim 6, Yamane shows in figure 1, a circuit for detecting and correcting clocking errors in the synchronization of a DTE data signal with a DCE clocking signal in a communication environment wherein the DCE interfaces the DTE to a communication channel, the circuit comprising:

p. Means for producing a master clock signal (Yamane fig. 4: phi0)

q. Means for deriving a ~~circuit~~ DCE clocking signal (Yamane fig. 4: phi1) and an internal clocking signal (Yamane fig. 4: phi2) from said master clocking signal, said ~~circuit~~ internal clocking signal (Yamane fig. 7: phi2) having the same frequency as the DCE clocking signal (Yamane fig. 7: phi1)

r. Means for obtaining a first sample of said DTE data signal at a first time ~~based on said circuit clocking signal~~ (Yamane fig. 11m: D(0)) ~~and obtaining~~ a second sample of said DTE data signal at a second time ~~based on said master clocking signal~~ (Yamane fig. 11m: D(1)), said second time being subsequent to said first time (Yamane fig. 11m: D(1) is after D(0)), the time interval between said first time and said second time being less than the period of the DCE clocking signal (Yamane fig. 11 m, n, d: the clock for clocking the MD1 data in m is in n which is at twice the frequency of the divided clock, d, which is the DCE clocking signal phi1)

s. Means for comparing said first sample to said second sample (Yamane fig. 8: comparison of samples is occurring in 31 with the NAND gates)

t. means for generating a selector control signal if said first sample is different from said second sample (sample comparator (Yamane fig. 10: 49) generates a selector control signal (Yamane fig. 1: outputs of 49) if said first sample (Yamane fig. 10: 49: output of the NAND gate through with D1 is input) is different from said second sample (Yamane fig. 10: 49: output of the NAND gate through with D2 is input).)

u. (103) means for inverting said ~~circuit~~ internal clocking signal to produce an inverted ~~circuit~~ clocking signal (an inverter (Yamane fig. 10: combination of buffer 54 and delay 51 produce an inverter) producing an inverted circuit clocking signal (Yamane fig. 11d is normal phi1 and 11f is inverted phi1) from said circuit clocking signal (Yamane fig. 11d: phi1; fig. 10: phi1); since phi1 is inverted, it would be obvious to make phi2 inverted since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. In re Einstein, 8 USPQ 167 and

since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.); and

v. means for selecting, in response to said selector control signal, an output signal from the group consisting of said ~~circuit~~ internal clocking signal and said inverted circuit clocking signal (not in Yamane)

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Monday through Thursday after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on (703) 305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3800.

PK
January 15, 2003

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 1/21/03